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HANDS-ON RADIO

Experiment 97

Programmable Frequency Reference

A recent article in the NZART *Break-In* magazine reminded me that a frequency reference was once part of every ham's shack, using a stable oscillator based on a 100 kHz (or 1 MHz) crystal.¹ The oscillator's fundamental and harmonics were used to identify the various band and segment edges. Although modern commercial gear may not need a frequency reference, what of the homebrew rig? With that in mind, this month's experiment uses a multistage counter to create a programmable reference for calibration or alignment or for generating a digital clock signal.

The Ripple Counter

Ripple counters were introduced in Hands-On Radio Experiment #36 — The Up-Down Counter.² Because they are asynchronous, the ripple counter isn't a very good choice for keeping a consistent count of input events because the change of state propagates (or ripples) through the chain of flip-flops. As a result it takes some time for the counter to stabilize after each count.

In our application, asynchronous operation is not an issue. It's only important that the counter has enough stages to divide the input signal by a large enough number. (There is one caveat we'll discuss at the end.)

We're going to use the 74HC4040 12 stage ripple counter. Enter 74HC4040 DATA SHEET into an Internet search engine and download a copy for reference. The internal circuit of the IC consists of *toggle flip-flops* that change the state of their Q and \bar{Q} outputs whenever the T input changes from low to high. Figure 1 shows the logic diagram. The *truth table* for the counter is shown in Table 1.

The data sheet should also provide a *timing diagram* of the relationship between the control, input and output signals. The 74HC4040 has one control input — the master reset at pin 11 connected to the R_D

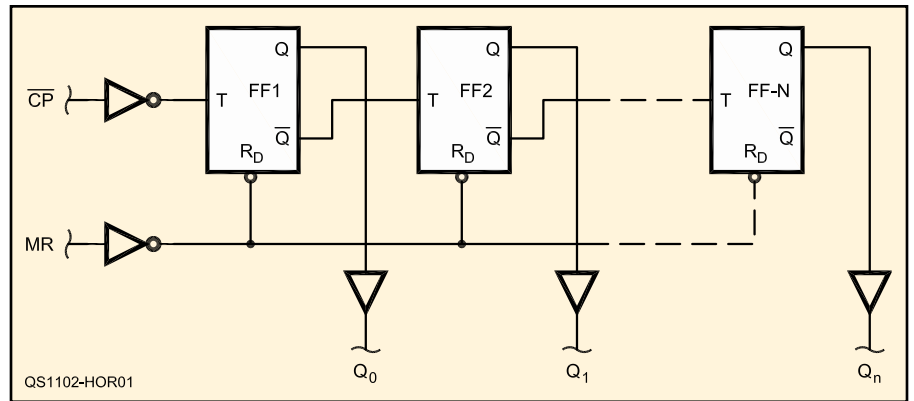


Figure 1 — The internal logic diagram of the 74HC4040 counter IC.

Table 1
Function Table of 74HC4040 Counter IC

Inputs		Outputs
CP	MR	Q_n
↑	L	No Change
↓	L	Count
x	H	L

Notes:

- H = High voltage level.
- L = Low voltage level.
- x = Don't care.
- ↑ = Low to high voltage transition.
- ↓ = High to low voltage transition.

input of each flip-flop — and one signal input — the clock pulse at pin 10. (MR and CP on the Philips data sheet, respectively.) If MR is high, all of the flip-flops are forced to the state in which Q is low and \bar{Q} is high, regardless of what \bar{CP} is doing. You can see this in the timing diagram because no flip-flop changes state until MR is low.

Once MR is released, the next high to low transition of the \bar{CP} signal causes the first flip-flop's Q output to go high and the \bar{Q} output to go low. Each successive high to low \bar{CP} transition causes the first flip-flop's Q and \bar{Q} outputs to change state. No action occurs if the \bar{CP} input changes from low to high. Since the \bar{Q} output of one stage is the input to the following stage, each flip-flop

changes state at $\frac{1}{2}$ the rate of the preceding flip-flop.

The counter's outputs Q_0 to Q_{11} produce a square wave with a frequency of the input divided by powers of 2 from $2^1 = 2$ to $2^{12} = 4096$, respectively. The counter advances from 0 (all Q outputs low) to 4095 (all Q outputs high) and then returns to 0 for a total of 4096 states.

If our objective were to divide the input signal by any integer power of 2, our work would be done — use the output corresponding to that ratio. Generally we want some other divisor than a power of two and that's where the fun begins.

Getting Wired

The function of the row of diodes and the JK flip-flop labeled U2A in Figure 2 is to detect that the counter has reached a specific count (N) and reset the counter to zero. Imagine that the shorting jumpers labeled J0 to J11 are all installed. Thus, all of the diode anodes share a common connection to the 4.7 k Ω pull-up resistor. Since each cathode is connected to a Q output, if any Q output is low the current through that diode will pull the anode connection low. For the anode connection to be high, all of the Q outputs must also be high. This is a wired-AND connection — all of the inputs to the wired-AND (the counter outputs) must be high for the output (the anode connection) to be high. (If the diodes were turned around, exchanging

¹A. Woodfield, ZL2PD, "Programmable CMOS Clock Generator," *Break-In*, New Zealand Association of Radio Transmitters, Sep/Oct 2009, pp 6-7.

²All previous Hands-On Radio experiments are available to ARRL members at www.arrrl.org/hands-on-radio.

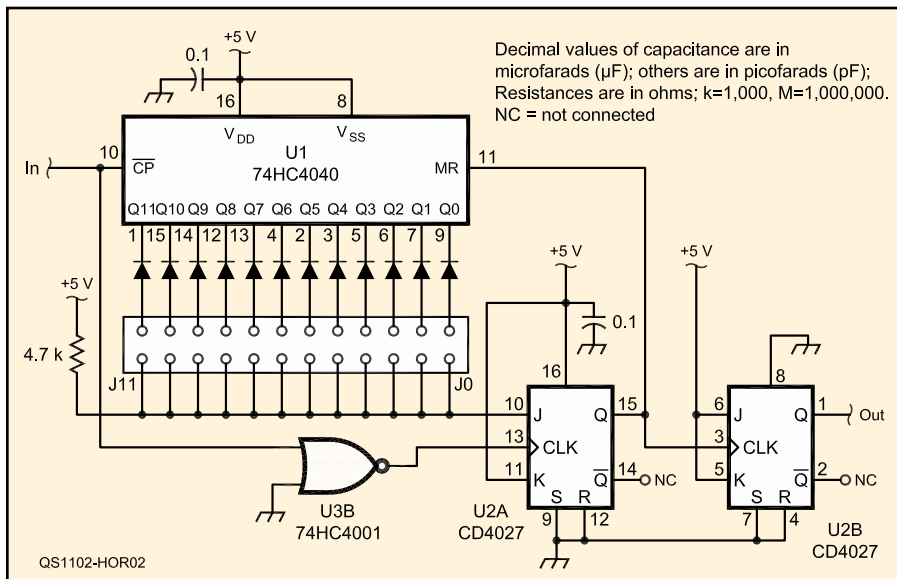


Figure 2 — The counter U1 and wired-AND circuit divide the input signal frequency by up to 4096. The output of U2A is a reset pulse at the frequency of the counter output. U2B divides the reset pulse frequency by two, creating a symmetrical square wave. J0 to J11 can be wire jumpers, a header strip with removable jumpers or DIP switch arrays.

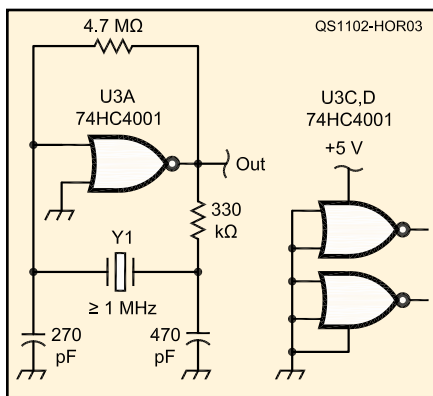


Figure 3 — A crystal oscillator circuit for high frequency and tuning fork crystals. For tuning fork crystals, replace 270 pF with 10 pF and 470 pF with 47 pF.

the anode and cathode, that would be a wired-OR connection for which the output would be high if any of the inputs were high.)

The wired-AND connection forms our *count detector* used to reset the counter and control the ratio of frequency division. We can make the wired-AND output go high after the desired count is reached by using the jumpers to select which counter outputs are connected to the wired-AND. Here's how it works: Say that we want U1 to divide the counter's input clock by 35. First, convert 35 to a 12 bit binary number with one digit for each counter output: 000000100011B (the right-most B denotes a binary number) with Q₁₁ corresponding to the *most significant bit* (MSB) on the left and Q₀ to the *least significant bit* (LSB) on the right. This describes the counter outputs after 35 low to high transitions of the input signal: Q₀, Q₁ and Q₅

are high and all the rest are low.

If these three jumpers (J0, J1 and J5) are connected and the other jumpers disconnected, the wired-AND will go high as the count of 35 is reached. The other jumpers are not connected because we don't want the wired-AND to go high at any other count but 35. When 35 is reached that is the first time the combination of counter outputs will cause the wired-AND to go high. It doesn't matter if any higher count causes Q₀, Q₁ and Q₅ to be high (such as 37, 39, etc) because the counter will not reach those values.

The wired-AND output is the J input to the flip-flop U2A, so the Q output of U2A will go high at the following low to high transition of the input signal at U2A's clock input. (The input signal is inverted by U3B, a NOR gate wired as an inverter, so that it acts at the same time as the ripple counter's clock.) U2A's \bar{Q} output is also connected to U1's reset input, causing all of the flip-flop Q outputs, the wired-AND output, and U2A's J input to go low. At the next input signal low to high transition, one input cycle later, U2A's Q output returns to low, creating a pulse one input signal cycle long. The pulse occurs every 35 counts, so the input frequency has been divided by 35!

Squaring the Cycle

We could stop here, but if we are going to use the circuit as a frequency reference, it would be preferable to have a symmetrical output. That is the function of U2B, the other half of the 74HC4027. This flip-flop divides its input signal frequency by two, producing a square wave. So, if the jumpers are set to divide the input frequency, f_{in} , by N, the circuit's output frequency will be $f_{in} / 2N$. The

sharp edges of the 74HC series logic signals are rich in harmonics, making an especially good *marker generator* for a homebrew receiver. If you do intend to use the circuit as a receiver calibrator use a metal enclosure, filter the input power well, and connect only the output signal to a short antenna.

The caveat regarding the ripple counter's asynchronous operation involves propagation delay through the counter as compared to the shortest input cycle period. For the circuit of U2A to function properly, its J input must be high *before* its clock input signal's low to high transition. Since the J input won't be high until the most significant ripple counter output connected to the wired-AND goes high, the total propagation delay through the ripple counter must be *less* than input signal period or a reset pulse won't be generated. Using typical values for propagation delay from the CLOCK input to Q_n at power supply voltages of 4.5 V, it takes $17 + 11 \times 10 = 127$ ns from the input for Q₁₁ to change. That puts an upper limit of $1 / 127$ ns = 7.87 MHz on the input signal if the Q₁₁ output is to be used, although the limit is higher with lower values of N.

Figure 3 shows an oscillator circuit that can be used for crystals above a few hundred kHz and for tuning fork crystals that operate at 32 kHz or lower. You can use any input signal as long as it meets the 74HC4040 requirements for logic high and low levels. Crystal manufacturers usually publish application notes showing how to make an oscillator at any frequency.

Parts List

- 74HC4001 — quad NOR gate IC.
- CD4027 IC — dual D type flip-flop IC.
- 74HC4040 — 12 stage ripple counter IC.
- 12 — 1N4148 signal diodes.
- 2 — 100 nF capacitor.
- 270 pF and 470 pF capacitors (assuming high-frequency crystal).
- 4.7 kΩ, 330 kΩ and 4.7 MΩ resistors.

Recommended Reading

The ARRL Handbook's updated "Digital Basics" chapter has a good discussion of counters and other digital concepts.³ Your library may have the terrific *CMOS Cookbook* on the shelves, as well, with many other great counter circuits.⁴

³*The ARRL Handbook for Radio Communications*, 2011 Edition. Available from your ARRL dealer or the ARRL Bookstore, ARRL order no. 0953 (Hardcover 0960). Telephone 860-594-0355, or toll-free in the US 888-277-5289; www.arrl.org/shop; pubsales@arrl.org.

⁴D. Lancaster, rev by H. Berlin, *CMOS Cookbook*, Howard W. Sams & Company, 1988.

